

Amendment to the Claims:

This listing of claims will replace all prior versions, and listing, of claims in the application.

Listing of Claims:

1. (currently amended) A method for performing Printed Circuit Board (PCB) panel optimization, comprising the steps of:

performing a panel dimension loop that goes through a plurality of possible panel dimensions;

performing an array length loop that goes through a plurality of array lengths;

performing an array width loop that goes through a plurality of array widths;

and

calculating a panel efficiency factor for each iteration of each of the loops ~~in order to determine a panel layout; and~~

adjusting a panel layout based on an optimum calculated panel efficiency.

2. (original) A method as defined in claim 1, further comprising the step of:

preparing initial data regarding panel dimension range, minimum and maximum array length and minimum and maximum array width.

3. (original) A method as defined in claim 2, wherein the initial data is used to limit the amount of iterations that are performed by the panel dimension loop, the array length loop and the array width loop.

4. (original) A method as defined in claim 2, wherein the step of preparing the initial data further comprises preparing initial data on PCB and array spacing requirements, array and panel border requirements and PCB outlines.

5. (original) A method as defined in claim 1, wherein for each iteration of the panel dimension loop as many arrays are fitted onto the panel as possible.

6. (original) A method as defined in claim 1, further comprising the step of:
applying array spacing and panel border specification requirements.

7. (original) A method as defined in claim 6, further comprising the steps of:
comparing the panel efficiency factors for each iteration; and
selecting the highest panel efficiency factor and using its corresponding panel dimension and array size for the panel layout.

8. (original) A method as defined in claim 7, further comprising the step of:
performing a sensitivity analysis in which outputs can be provided regarding possible changes to any one or more of the panel dimensions, array size, array spacing and panel border specification requirements.

9. (original) A method as defined in claim 2, wherein the step of preparing the initial data comprises inputting data using a web based graphical user interface.

10. (original) A method as defined in claim 9, wherein the step of preparing the initial data further comprises importing an outline file of a PCB that is to be fitted into the arrays and panel.

11. (original) A method as defined in claim 10, wherein the outline file of the PCB provides information on a complex polygon that defines the PCB that is to be fitted into the arrays.

12. (currently amended) A method for optimizing the fitting of Printed Circuit Boards (PCBs) onto at least one array and the at least one array onto a PCB panel, the method comprises the steps of:

loading information regarding the outline of the PCBs;
performing multiple iterations regarding different potential dimensions for the panel and the at least one array; and
determining a Panel Efficiency Factor (PEF) for each iteration ~~in order to~~
~~determine the array and panel dimensions to use for the particular PCB outline.; and~~
generating a PCB outline utilizing the PEF iterations to determine optimum array and panel dimensions.

13. (original) A method as defined in claim 12, wherein the information regarding the outline of the PCBs is automatically imported from a design file which provides information on a complex polygon that defines the PCB outline.

14. (original) A method as defined in claim 12, further comprising the steps of:
inputting information regarding panel dimensions that can be used and the minimum and maximum array length and width that can be used; and
using the information inputted to determine the array and panel dimensions.

15. (original) A method as defined in claim 14, wherein in the inputting step, information regarding PCB and array spacing requirements and array and panel border requirements are also inputted and used to determine the array and panel dimensions.

16. (original) A method as defined in claim 15, wherein in the inputting step, information regarding whether the PCBs can be rotated in the at least one array during the fitting of the PCBs onto the at least one array is entered.

17. (original) A method as defined in claim 12, wherein the array and panel dimensions are determined by selecting the array and panel dimension combination that provides for the highest PEF.

18. (original) A method as defined in claim 17, wherein the method is performed using a web based software tool that includes a graphical user interface.

19. (original) A method as defined in claim 17, wherein if more than one array and panel dimensions yields the highest PEF, the one having the largest array size is selected as the panelization solution.